

## **CURRICULUM VITAE**

**KODIGUDLA DEEPTHI**

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### **Career Objective**

Pursue higher status in an Esteemed Organization and to be a part of Innovative environment which will provide me mutual growth and development.

### **Strengths**

Comprehensive problem-solving abilities, Ability to deal with people diplomatically.

### **Academic Profile**

<b>Class</b>	<b>University/Board</b>	<b>Year of Study</b>	<b>College/Institution</b>	<b>Percentage</b>
M.Tech VLSI	Autonomous	2017-2019	MVGR College of Engineering	9.42(CGPA)
B.Tech ECE	Jntu Kakinada	2012-2016	Avanthi Institute of Engineering and Technology	73.33
Intermediate MPC	Board of Intermediate Education	2010-2012	Narayana Junior College	80.06
Xth Class	ICSE Syllabus	2000-2010	St. Joseph's Girls High School	61.3

## Experience

- I am working as an Assistant Professor in Electronics and Communication Department of Avanthi institute of engineering and Technology College since January 23<sup>th</sup>.2023 to till date.
- I am worked as Assistant Professor in Electronics and Communication Department of Avanthi institute of engineering and Technology College since February 15<sup>th</sup> 2021 to January 20<sup>th</sup> 2023.
- I worked as Guest Lecturer in Electronics and Communication Department of Andhra University for Women's engineering college Since July 1<sup>st</sup> 2019 to March 15<sup>th</sup> 2020.

## Achievements

- Announced **JNTUK Pratibha Awards 2019** for securing highest percentage of marks in M.Tech ECE VLSI specialization.

## Internship

- NPTEL online course done in **Accreditation and outcome Based Learning** and secured 80% in 2023.
- **UHV-I** Courses completed in the year of 2022
- NPTEL online course done in **Research Methodologies** and secured 70% in 2019.
- Done my internship at **Steel Plant** in **Telecommunications Dept,** Visakhapatnam (June 2015- July 2015)

## Technical Skills

- Programming Languages : C
- Simulation Tools : Mplab ,Mentorgraphic layout design.
- Platforms : Microsoft Windows.
- Hardware skills : Installation.

## **Publications**

**Published** a paper entitled “**DESIGN OF 18-TRANSISTOR TSPC FLIP-FLOP BASED ON LOGIC STRUCTURE REDUCTION SCHEMES**” in **International Journal of Research ( Impact Factor 5.7)** , Volume V III, Issue V ,May 2019.

## **Training and seminars**

- Attended Ten-day NEP-2020 Orientation and sensitization Programme under Malaviya Mission Teacher Training Programme development program organized by UGC –MMTTC Andhra University, Visakhapatnam
- Attended five-day faculty development program on “opportunities and challenges in next generations semiconductors devices” organized by Anil Neerukonda institute of technology and sciences, Visakhapatnam
- Attended a seven-day national level faculty development program on “online teaching-learning processes using ICT tool of education 4.0” organized by ST. Vincent pallotti college of engineering g and technology, Nagpur
- Participated in the webinar on “meandering of specialization” organized by Mahendra college of engineering, Chennai.
- Participated in the webinar on “VLSI layout design using mentor graphics tool” conducted by Pantech E BYTES

## **Personal Skills**

- Ability to take up responsibilities.
- Able to maintain interpersonal skills.

## Personal Profile

- Name : K.Deepthi
- Father's Name : K.BhaskarRao
- Mother's Name : K.Uma
- Date Of Birth : 15-09-1994
- Sex : Female
- Marital Status : married

## Declaration

If given a chance to work in your organization, I assure the best of my services to the organization and reach up to the expectations of my superiors.

Date:

Place: Visakhapatnam.

(K. DEEPTHI)