RESUME

Venkateshseerapu
Latchayyapeta,
Seethanagaram (Mandal),
Vizianagaram (Dist),
Andhra Pradesh.
PIN: 535573

Email Id: venkateshseerapu2019@gmail.com
Mobile No: 9666594294

Career Objective:

To work with a professional managed organization where I can take challenges in order to widen my career horizons and contribute my best for the progress of organization.

Academic Qualifications:

Class	Discipline/ Specialization	Board/ University	Institution	Year of passing	% of Marks
Ph.D. (Pursuing)	VLSI	Andhra University	Andhra University	-	-
M.Tech	VLSI	JNT University, Kakinada	MVGR college of engineering	2012	75.64
B.Tech	Electronics & Communication Engineering	JNT University, Kakinada	Gokul Institute of Technology and sciences	2009	70.99
Intermediate	M.P.C	Board of Intermediate Education	Sai Vikas Junior College	2005	82.6
X Class	S.S.C	Board of Secondary Education	Abhyudaya Convent & High School	2003	85

Experience:

- Presently Working as Asst. Professor in **Gayatri Vidya Parishad College for Degree and PG Courses, School Of Engineering, Visakhapatnam** from 16/06/2014 to till date
- Worked as Asst. Professor in **VITS Group of Institutions, Visakhapatnam** from 28/11/2012 to 10/06/2014.

Technical Skills:

- Designing Software: Mentor Graphics, LabVIEW, MATLAB, Tanner Tools, Xilinx, Spice Software's.

Academic Projects:

- **B.Tech Project:**

  Accident Identification Using GPS & GSM

- **M.Tech Project:**

  Implementation of Optimized Reconfigurable Built In Self Repair Scheme For RAM's In SOC

Workshops attended:

- Participated in One Week FDP Course on **Low Power VLSI Design for Communication Systems and Networks** organized by **Dr. B R Ambedkar National Institute of Technology, Jalandhar** from 16-09-2020 to 20-09-2020.

- Participated in Three days FDP Course on **Antenna Design and Analysis using FEKO** organized by **Gayatri Vidya Parishad College for Degree and PG Courses (A)** from 22.06.2020 to 24.06.2020.

- Participated in One Week FDP Course on **Recent trends in VLSI** organized by **Gokaraju Rangaraju Institute of Engineering And Technology** from 02.06.2020 to 07.06.2020.

- Participated in Three days FDP Course on **Research Topics in VLSI and Industry Trends** organized by **GMRIT** from 29.05.2020 to 31.05.2020.

- Participated in One Week FDP Course on **IoT** organized by **Andhra Pradesh State Skill Development Corporation (APSSDC)** from 18.05.2020 to 30.05.2020.

- Participated in Two Day Training Program on **IIC Innovation Ambassador Training Program** at **MLR Institute of Technology** from 06.02.2020 to 07.02.2020.

- Participated in Two Day Workshop on **Learning Management System** at GVP **College for Degree and PG Courses (A)** from 30th April to 1st May 2019.

- Participated in Two Day Workshop on **Learning Management System** at GVP **College for Degree and PG Courses (A)** from 30th April to 1st May 2019.

- Participated in a three day workshop on **Custom Analog and Digital IC Design using Mentor EDA Tools** at **GVP college of engineering for women** from 27th to 29th September 2018

- Participated in a **Two-Week ISTE STTP on CMOS, Mixed Signal and Radio Frequency VLSI Design** conducted by **IIT Kharagpur** from 30th Jan 2017 to 4th Feb 2017.

- Worked as a co-convener in two day international conference **ICRIESHM-2016** at GVP College for degree and PG courses, school of engineering.

- Participated in a three day national workshop on **Analog and Digital Circuit Design using CADENCE** at GVP college of engineering

- Participated in a two day national workshop on VLSI & EDA TOOLS at JNTU, vizianagaram.

- Participated in a three day faculty development programme conducted by Dr. B.G. Barki, Retd. Professor of education NITTTR, Chennai at VITS Group of Institutions.

- Participated a three day faculty development programme on **Outcome-Based Engineering Education for Employability Enhancemen**t at VITS Group of Institutions.

- Participated in a Workshop on **LABVIEW Technologies** at MVGR College of engineering.

- **Digital Communication Faculty Development Program Conducted By APSCHE** in MVGR College of engineering.

- **WOLTEC (Workshop on Latest Technologies in Electronics and Communications)** at MVGR College of engineering.

- **Xilinx** workshop at GVP College of engineering.

Publications:

1. S. Venkatesh[1] , K. Pavankumar[2] , K. Saikiran Reddy[3] , P. Praveen Kumar[4] , G. Venkatesh[5], "***Leakage Reduction in 180nm CMOS Full Adder using Modified Lector Technique***" published at: **International Journal for Research in Applied Science & Engineering Technology (IJRASET)**, Volume 7 Issue IV, Apr 2019- Available at www.ijraset.com.

2. Venkatesh Seerapu1, N Sowmya2 and Priyanka Palaka3, "***Dynamic Power Reduction in Digital VLSI Circuits Using Stacked LCNMOS***" published at: **International Journal of Advanced Research inScience and Technology**, Volume 7, Issue 1, 2018, pp. 757-760 .

3. S. Venkatesh, N. Sowmya, S. Krishna Veni "**Design of Low Power Multiplier Using Modified Reversible Logic Gate"** published at: **GVP Journal Of Science Technology And Management,** Volume 1, Issue 1-2017

4. G Amitha, M Chandra sekhar, D Santosh, Venkatesh S – "***An Area Efficient Reversible Multiplier Circuit Design By Using Low power Technique***" published at: **International Journal of Engineering Research and Applications (IJERA**) ISSN: 2248-9622 www.ijera.com Vol. 3, Issue 2, March -April 2013, pp.1819-1824.

5. BagadiMadhavi, G Kanchana, SeerapuVenkatesh – ***Low Power and Area Efficient Design of VLSICircuits*** – published at: "**International Journal of Scientific and Research Publications (IJSRP)**, Volume 3, Issue 4, April 2013 Edition".

6. Venkatesh S, LaxmiPrasanna Rani M, " **Implementation Of Optimized Reconfigurable Built-In Self-Repair Scheme For Rams In Socs**" etal, **(IJCSIT) International Journal Of Computer Science And Information Technologies**, Vol. 3 (3) , 2012, 4443 – 4446.

Professional Bodies Membership:

- Member of International Association of Engineers with Id: 232386
- Member of IFERP with Id: PMIN40392785

Achievements:

- Qualified for Assistant Professor in UGC-NET June, 2019.
- Ratified as Assistant Professor by Andhra University.
- Qualified in GATE-2016.
- Qualified in GATE-2013.
- Received prize in B.Tech for being topper in academics.

Strengths:

- Smart Working
- Time managing skills
- Adaptability

Personal Details:

Father's Name	:	S.Krishnarao
Date of Birth	:	10th June 1988
Marital Status	:	SINGLE
Religion	:	Hindu
Nationality	:	Indian
Sex	:	male
Languages Known	:	English, Telugu

DECLARATION

I hereby declare that all statements made above are true, complete and correct to the best of my knowledge and belief.

Date:

Place: Visakhapatnam. S.Venkatesh